

a memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

1 2. (Unchanged) The computer system of claim 1, wherein the refresh timing circuit
2 triggers memory refresh events whenever the computer system is operating in a normal
3 mode and a low power mode.

1 3. (Unchanged) The computer system of claim 2, wherein the refresh timing circuit
2 further comprises:

3 a clock generator for generating the clock pulses;
4 a first counter coupled to the clock generator;
5 a storage register coupled to the clock generator and the counter; and
6 a comparator coupled to the clock generator, the counter and the storage
7 register.

1 4. (Unchanged) The computer system of claim 3, wherein the first counter counts
2 the number of clock pulses generated by the clock generator.

1 5. (Unchanged) The computer system of claim 4, wherein the first counter transmits
2 data to the storage register whenever the computer system is operating in the normal
3 mode, the data representing the number of clock pulses counted by the counter since the
4 occurrence of a prior memory refresh event.

1 6. (Unchanged) The computer system of claim 5, wherein the storage register
2 transmits the data to the comparator upon a transition from the normal mode to the low
3 power mode.

1 7. (Unchanged) The computer system of claim 6, wherein the first counter transmits
2 signals to the comparator whenever the computer system is operating in the low power
3 mode, the signal representing the number of clock pulses received from the clock
4 generator.

1 8. (Unchanged) The computer system of claim 7, wherein the comparator compares
2 the signal received from the first counter and the data received from the storage register,
3 and wherein the comparator transmits a refresh trigger signal whenever there is a match
4 between the signal and the data.

1 9. (Unchanged) The computer system of claim 4, wherein the refresh timing circuit
2 further comprises a second counter.

1 10. (Unchanged) The computer system of claim 9, wherein the first counter counts
2 the number of clock pulses generated by the clock generator while the computer system is
3 operating in the low power mode and the second counter counts the number of clock
4 pulses generated by the clock generator while the computer system is operating in a
5 normal mode.

1 11. (Unchanged) The computer system of claim 10, wherein the second counter
2 transmits data to the storage register upon the occurrence of a memory refresh event
3 whenever the computer system is operating in the normal mode, the data representing the
4 number of clock pulses counted by the counter since the occurrence of a previous memory
5 refresh event.

1 12. (Unchanged) The computer system of claim 11, wherein the second counter is
2 deactivated and the first counter is activated whenever the computer system transitions
3 from the normal mode to the low power mode.

1 13. (Unchanged) The computer system of claim 12, wherein the first counter
2 transmits signals to the comparator whenever the computer system is operating in the low
3 power mode, the signal representing the number of clock pulses received from the clock
4 generator.

1 14. (Unchanged) The computer system of claim 3, wherein the refresh timing circuit
2 includes a second counter for triggering memory refresh events whenever the computer
3 system is operating in the normal mode

1 15. (Unchanged) The computer system of claim 1, wherein the memory is an
2 Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory
3 controller is an EDO DRAM controller.

1 16. (Amended) A memory controller comprising:
2 a refresh timing circuit for generating clock pulses used to trigger memory
3 refresh events.

1 17. (Amended) The memory controller of claim 16, wherein the refresh timing
2 circuit further comprises:

3 a clock generator;
4 a first counter coupled to the clock generator;
5 a storage register coupled to the clock generator and the counter; and

AI 6 a comparator coupled to the clock generator, the counter and the storage
7 register.

1 18. (Amended) The memory controller of claim 17, wherein the memory controller
2 operates in a normal mode and a low power mode.

1 19. (Amended) The memory controller of claim 18, wherein the first counter counts
2 the number of clock pulses generated by the clock generator.

1 20. (Amended) The memory controller of claim 19, wherein the first counter
2 transmits data to the storage register whenever the memory controller is operating in the
3 normal mode, the data representing the number of clock pulses counted by the counter
4 since the occurrence of a previous memory refresh event.

1 21. (Amended) The memory controller of claim 20, wherein the storage register
2 transmits the data to the comparator upon a transition from the normal mode to the low
3 power mode.

1 22. (Amended) The memory controller of claim 21, wherein the first counter
2 transmits signals to the comparator whenever the memory controller is operating in the
3 low power mode, the signal representing the number of clock pulses received from the
4 clock generator.

1 23. (Amended) The memory controller of claim 22, wherein the comparator
2 compares the signal received from the first counter and the data received from the storage
3 register, and wherein the comparator transmits a refresh trigger signal whenever there is a
4 match between the signal and the data.

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1 24. (Amended) The memory controller of claim 19, wherein the refresh timing
2 circuit further comprises a second counter.

1 25. (Amended) The memory controller of claim 24, wherein the first counter counts
2 the number of clock pulses generated by the clock generator while the memory controller
3 is operating in the low power mode and the second counter counts the number of clock
4 pulses generated by the clock generator while the memory controller is operating in the
5 normal mode.

1 26. (Amended) The memory controller of claim 25, wherein the second counter
2 transmits data to the storage register upon the occurrence of a memory refresh event
3 whenever the memory controller is operating in the normal mode, the data representing the
4 number of clock pulses counted by the counter since the occurrence of a previous memory
5 refresh event.

1 27. (Amended) The memory controller of claim 26, wherein the second counter is
2 deactivated and the first counter is activated whenever the memory controller transitions
3 from the normal mode to the low power mode.

1 28. (Amended) The memory controller of claim 27, wherein the first counter
2 transmits signals to the comparator whenever the memory controller is operating in the
3 low power mode, the signal representing the number of clock pulses received from the
4 clock generator.

Please add the following new claims:

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1 38. (New) A refresh timing circuit comprising:

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2 an internal clock generator;
3 a first counter coupled to the clock generator;
4 a storage register coupled to the clock generator and the counter; and
5 a comparator coupled to the clock generator, the counter and the storage
6 register.

1 39. (New) The refresh timing circuit of claim 38, wherein the refresh timing circuit
2 operates in a normal mode and a low power mode.

1 40. (New) The refresh timing circuit of claim 39, wherein the first counter counts the
2 number of clock pulses generated by the clock generator.

1 41. (New) The refresh timing circuit of claim 40, wherein the first counter transmits
2 data to the storage register whenever the refresh timing circuit is operating in the normal
3 mode, the data representing the number of clock pulses counted by the counter since the
4 occurrence of a previous memory refresh event.

1 42. (New) The refresh timing circuit of claim 41, wherein the storage register
2 transmits the data to the comparator upon a transition from the normal mode to the low
3 power mode.

1 43. (New) The refresh timing circuit of claim 42, wherein the first counter transmits
2 signals to the comparator whenever the refresh timing circuit is operating in the low power
3 mode, the signal representing the number of clock pulses received from the clock
4 generator.

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1 44. (New) The refresh timing circuit of claim 43, wherein the comparator compares
2 the signal received from the first counter and the data received from the storage register,
3 and wherein the comparator transmits a refresh trigger signal whenever there is a match
4 between the signal and the data.

1 45. (New) The refresh timing circuit of claim 40, further comprising a second counter.

1 46. (New) The refresh timing circuit of claim 45, wherein the first counter counts the
2 number of clock pulses generated by the clock generator while the refresh timing circuit is
3 operating in the low power mode and the second counter counts the number of clock
4 pulses generated by the clock generator while the refresh timing circuit is operating in the
5 normal mode.

1 47. (New) The refresh timing circuit of claim 46, wherein the second counter
2 transmits data to the storage register upon the occurrence of a memory refresh event
3 whenever the refresh timing circuit is operating in the normal mode, the data representing
4 the number of clock pulses counted by the counter since the occurrence of a previous
5 memory refresh event.

1 48. (New) The refresh timing circuit of claim 47, wherein the second counter is
2 deactivated and the first counter is activated whenever the refresh timing circuit
3 transitions from the normal mode to the low power mode.

1 49. (New) The refresh timing circuit of claim 48, wherein the first counter transmits
2 signals to the comparator whenever the refresh timing circuit is operating in the low

A2 3 power mode, the signal representing the number of clock pulses received from the clock
4 generator.
